Reducing the Jitters

How a Chip-Scale Atomic Clock Can Help Mitigate Broadband Interference

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THE GLOBAL POSITIONING SYSTEM IS A MARVEL OF SCIENCE AND ENGINEERING. It has become so ubiquitous that we are starting to take it for granted. Receivers are everywhere. In our vehicle satnav units, in our smart phones, even in some of our cameras. They are used to monitor the movement of the Earth's crust, to measure water vapor in the troposphere, and to study the effects of space weather. They allow surveyors to work more efficiently and prevent us from getting lost in the woods. They navigate aircraft and ships, and they help synchronize mobile phone and electricity networks, and precisely time financial transactions.

INNOVATION INSIGHTS
with Richard Langley

Atomic clocks can enhance the performance of GPS receivers.

GPS can do all of this, in large part, because the signals emitted by each satellite are derived from an onboard atomic clock (or, more technically correct, an atomic frequency standard). The signals from all of the satellites in the GPS constellation need to be synchronized to within a certain tolerance so that accurate (conservatively stated as better than 9 meters horizontally and 15 meters vertically, 95% of the time), real-time positioning can be achieved by a receiver using only a crystal oscillator. This requires satellite clocks with excellent long-term stability so that their offsets from the GPS system timescale can be predicted to better than about 24 nanoseconds, 95% of the time. Such a performance level can only be matched by atomic clocks.

The very first atomic clock was built in 1949. It was based on an energy transition of the ammonia molecule. However, it wasn't very accurate. So scientists turned to a particular energy transition of the cesium atom and by the mid-1950s had built the first cesium clocks. Subsequently, clocks based on energy transitions of the rubidium and hydrogen atoms were also developed. These initial efforts were rather bulky affairs but in the 1960s, commercial rack-mountable cesium and rubidium devices became available. Further development led to both cesium and rubidium clocks being compact and rugged enough that they could be considered for use in GPS satellites. Following successful tests in the precursor Navigation Technology Satellites, the prototype or Block I GPS satellites were launched with two cesium and two rubidium clocks each. Subsequent versions of the GPS satellites have continued to feature a combination of the two kinds of clocks or just rubidium clocks in the case of the Block IIR satellites.

While it is not necessary to use an atomic clock with a GPS receiver for standard positioning and navigation applications, some demanding tasks such as geodetic reference frame monitoring use atomic frequency standards to control the operation of the receivers. These standards are external devices, often rack mounted, connected to the receiver by a coaxial cable—too large to be embedded inside receivers.

But in 2004, scientists demonstrated a chip-scale atomic clock, and by 2011, they had become commercially available. Such small low-power atomic clocks can enhance the performance of GPS receivers in a number of ways, including enhanced code-acquisition capability that precise long-term timing allows. And, it turns out, such clocks can effectively mitigate wideband radio frequency interference coming from GPS jammers. We learn how in this month's column.

"Innovation" is a regular feature that discusses advances in GPS technology and its applications as well as the fundamentals of GPS positioning. The column is coordinated by Richard Langley of the Department of Geodesy and Geomatics Engineering, University of New Brunswick. He welcomes comments and topic ideas. To contact him, see the "Contributing Editors" section on page 6.

Currently installed Local Area Augmentation System (LAAS) ground receivers have experienced a number of disruptions in GPS signal tracking due to radio frequency interference (RFI). The main sources of RFI were coming from the illegal use of jammers (also known as personal privacy devices [PPD]) inside vehicles driving by the ground installations. Recently, a number of researchers have studied typical properties of popular PPDs found in the market and have concluded that the effect of PPD interference on the GPS signal is nearly equivalent to that of a wideband signal jammer, to which the current GPS signal is most vulnerable. This threat impacts LAAS or any ground-based augmentation system (GBAS) in two ways:

- Continuity degradation – as vehicles with PPDs pass near the GBAS ground antennas, the reference receivers lose lock due to the overwhelming noise power.
- Integrity degradation – the code tracking error will increase when the noise level in the tracking loop increases.

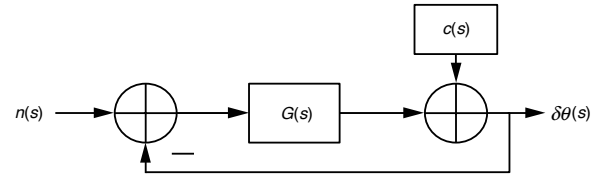
Numerous interference mitigation techniques have been studied for broadband interference. The interference mitigation methods can be separated according to the two fundamental stages of GPS signal tracking: the front-end stage, in which automatic gain control and antenna nulling/beam forming techniques are relevant, and the baseband stage, where code and carrier-tracking loop algorithms and aiding methods are applicable.

In our current work, the baseband strategy and resources that are

▲ **PHOTO** Chip-scale atomic clock.

practically implementable at GBAS ground stations are considered. Among those resources, we focus on using atomic clocks to mitigate broadband GNSS signal interference. For GPS receivers in general, wide tracking loop bandwidths are used to accommodate the change in signal frequencies and phases caused by user dynamics. Unfortunately, wide bandwidths also allow more noise to enter into the tracking loop, which will be problematic when wideband inference exists. The general approach to mitigate wideband interference is to reduce the tracking loop bandwidth. However, a reference receiver employing a temperature-compensated crystal oscillator (TCXO) needs to maintain a minimum loop bandwidth to track the dynamics of the clock itself, even when all other Doppler effects are removed. The poor stability of TCXOs fundamentally limits the potential to reduce the tracking loop bandwidth. This limitation becomes much less constraining when using an atomic clock at the receiver, especially in the static, vibration-free environment of a GBAS ground station.

Integrating atomic clocks with GPS/GNSS receivers is not a new idea. Nevertheless, the practical feasibility of such integration remained difficult until recent advancements in atomic clock technology, such as commercially available compact-size rubidium frequency standards or, more recently, chip-scale atomic clocks (CSACs). Most of the research using atomic clock integrated GPS receivers aims to improve positioning and timing accuracy, enhance navigation system integrity, or coast through short periods of satellite outages. In these applications, the main function of the atomic clock is to improve the degraded system performance caused by bad satellite geometries. As for using narrower tracking loop bandwidths to obtain better noise/jamming-resistant performance, the majority of work in this area has focused on high-dynamic user environments with extra sensor aiding, such as inertial navigation systems, pseudolites, or other external frequency-stable radio signals. These aids alone do not permit reaching the limitation of tracking loop bandwidth reduction since the remaining Doppler

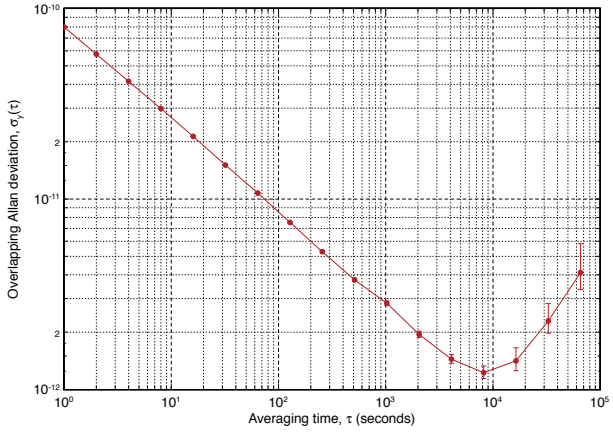


▲ **FIGURE 1** Simplified tracking loop diagram.

shift from user dynamics still needs to be tracked by the tracking loop itself. Our research intends to explore the lower end of the minimum tracking loop bandwidth for static GPS/GNSS receivers using atomic clocks.

High-frequency-stability atomic clocks naturally reduce the minimum required bandwidth for tracking clock errors (since clock phase random variations are much smaller). We have conducted analyses to obtain the theoretical minimum tracking loop bandwidths using clocks of varying quality. Carrier-phase tracking loop performance under deteriorated C/N_0 conditions (that is, during interference) was investigated because it is the most vulnerable to wideband RFI. The limitations on the quality of atomic clocks and on the receiver tracking algorithms (second- or third-order tracking loop bandwidths) to achieve varying degrees of interference suppression at the GBAS reference receivers are explored. The tracking loop bandwidth reductions and interference attenuations that are achievable using different qualities of atomic clocks, including CSACs and commercially available rubidium receiver clocks, are also discussed in this article.

In addition to the theoretical analyses, actual GPS intermediate frequency (IF) signals have been sampled using a GPS radio frequency (RF) frond-end kit, which is capable of utilizing external clock inputs, connected to a commercially available atomic clock. The sampled IF data are fed into a software receiver together with and without simulated wideband interference to evaluate the performance of interference mitigation using atomic clocks. The wideband interference is numerically



▲ **FIGURE 2** Allan deviations for chip-scale atomic clock.

simulated based on deteriorated C/N_0. The actual tracking errors generated from real IF data are used to validate the system performance predicted by the preceding broadband interference mitigation analyses.

Signal Tracking Loop and Tracking Error

The carrier-phase tracking phase lock loop (PLL) is introduced first to understand the theoretical connection between the carrier-phase tracking errors and the signal noise plus receiver clock phase errors. A simplified PLL is shown in FIGURE 1 with incoming signals set to zero. In the figure, $n(s)$, $c(s)$, and $\delta\theta(s)$ are receiver white noise, clock phase error or clock disturbance, and tracking loop phase error respectively, with s being the Laplace transform parameter. $G(s)$ is the product of the loop filter $F(s)$ and the receiver clock model $1/s$.

From Figure 1, the transfer functions relating the white noise and clock disturbance to the output can be derived as:

$$\frac{\delta\theta(s)}{n(s)} = \frac{G(s)}{1+G(s)} = H(s)$$
$$\frac{\delta\theta(s)}{c(s)} = \frac{1}{1+G(s)} = 1-H(s) \quad (1)$$

The frequency response of $H(s)$ is complementary to 1-$H(s)$. Therefore, the PLL tracking performance is a trade-off between the noise rejection performance and the clock disturbance tracking performance.

Total PLL errors resulting from different error sources are presented as phase jitter, which is the root-mean-square (RMS) of resulting phase errors. Equation (2) shows the definition of the standard deviation of phase jitter resulting from the error sources considered in this work:

$$\sigma_{\delta\theta} = \sqrt{\sigma_{\delta\theta,n}^2 + \sigma_{\delta\theta,c}^2 + \sigma_{\delta\theta,SV}^2} \quad (2)$$

where $\sigma_{\delta\theta,n}$, $\sigma_{\delta\theta,c}$, and $\sigma_{\delta\theta,SV}$ are standard deviations of receiver white noise, receiver clock errors, and satellite clock error, respectively, for static receivers.

The standard deviation for each of the clock error sources can be evaluated using the frequency reponse of the corresponding transfer function and power spectral densities (PSDs). The equations to evaluate the phase error from each error source are:

$$\sigma_{\delta\theta,n}^2 = \frac{B_w}{C/N_0}\left[1+1/(2\times T_c\times C/N_0)\right]$$
$$\sigma_{\delta\theta,c}^2 = \int_0^\infty |1-H(f)|^2 S_{rx}(f)df$$
$$\sigma_{\delta\theta,SV}^2 = \int_0^\infty |1-H(f)|^2 S_{SV}(f)df \quad (3)$$

Clock model	h_0	h_1	h_2	h_3	h_4
TCXO	5×10^{-8}	6.2×10^{-8}	9.6×10^{-8}	6×10^{-3}	6×10^{-4}
CSAC	5×10^{-8}	6.2×10^{-8}	1.6×10^{-6}	2.9×10^{-10}	6.1×10^{-12}
Rubidium	5×10^{-9}	6.2×10^{-9}	5.3×10^{-8}	0	1.2×10^{-17}

▲ **TABLE 1** Coefficients of power-law model.

where S_{rx} and S_{sv} are one-sided PSDs for receiver clock and satellite clock, respectively. B_w is the bandwidth of the tracking loop and T_c is the coherent integration time.

Receiver and Satellite Clock Models

In general, the receiver noise can be reasonably assumed to be white noise with constant PSD with magnitude (noise density) of N_0. However, it is not the case for clock errors. The clock frequency error PSD is usually formulated in the form of a power-law equation and has been used to describe the time and frequency behaviors of the random clock errors in a free running clock:

$$s_y(f) = h_{y0}f^2 + h_{y1}f^1 + h_{y2}f^0 + \frac{h_{y3}}{f} + \frac{h_{y4}}{f^2} \quad (4)$$

where $s_y(f)$ represents the PSD of clock frequency errors and is a function of frequency powers.

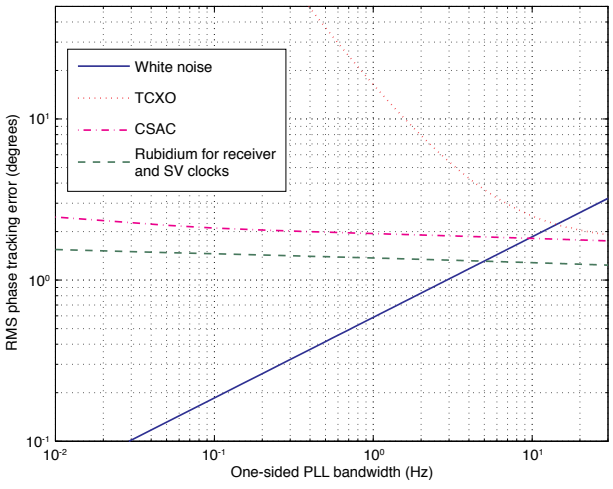
The clock phase error PSD can be analytically derived from the frequency PSD equation because the phase error is the time integral of the frequency error:

$$s_\varphi(f) = \left(\frac{f_0}{f}\right)^2 s_y(f)$$
$$= h_{y0}f_0^2 + h_{y1}\frac{f_0^2}{f} + h_{y2}\frac{f_0^2}{f^2} + h_{y3}\frac{f_0^2}{f^3} + h_{y4}\frac{f_0^2}{f^4}$$
$$= h_0 + \frac{h_1}{f} + \frac{h_2}{f^2} + \frac{h_3}{f^3} + \frac{h_4}{f^4} \quad (5)$$

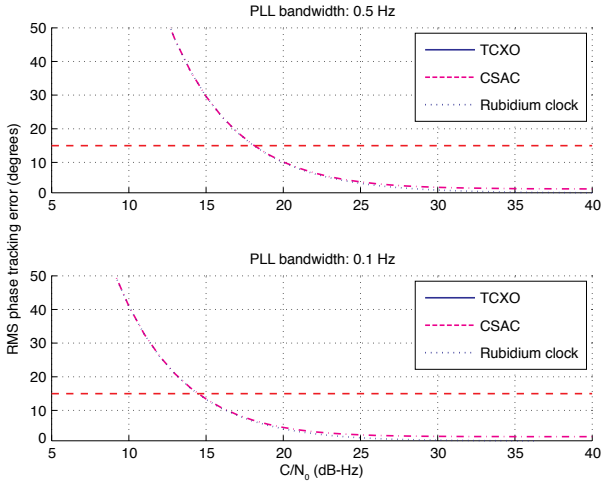
where f_0 is the nominal clock frequency. The h coefficients of the clock phase error PSD are the product of the h coefficients from the clock frequency error PSD and the nominal frequency.

We have adopted the PSD clock error models in our work to perform tracking loop performance analysis. The PSD of the CSAC is derived from an Allan deviation figure published by the manufacturer and is shown in FIGURE 2. We took three piecewise Allan deviation straight lines, which are slightly conservative, and converted them to a PSD.

Three PSDs of clock error models are listed in TABLE 1, which represent spectrums of the well known TCXO, the CSAC, and a rubidium standard. Phase noise related h_0 and h_1 coefficients in the CSAC model are assumed to be the same as the TCXO because they can't be obtained from the Allan deviation figure. The rubidium clock phase noises resulting from h_0 and h_1 coefficients are assumed to be two times smaller than those of the TCXO, and the



▲ **FIGURE 3** Phase error contribution from different error sources.



▲ **FIGURE 5** Tracking loop performance analysis for 0.5- and 0.1-Hz loop bandwidth.

same model is also used as the satellite clock error model in our tracking loop analysis.

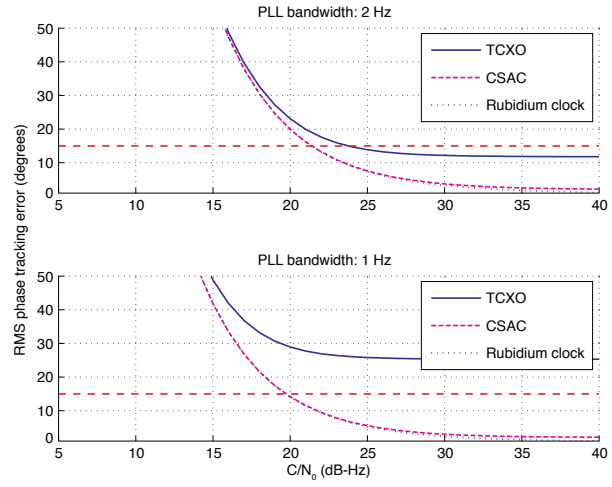
Theoretical Carrier Tracking Loop Performance

Second- and third-order PLLs are used to study the tracking loop performance. The loop filters for each PLL are given by:

$$F_2(s)=\frac{a_2 w_{0,2} s+w_{0,2}^2}{s},\quad F_3(s)=\frac{b_3 w_{0,3} s^2+a_3 w_{0,3}^2 s+w_{0,3}^3}{s^2} \qquad (6)$$

where $F_2(s)$ and $F_3(s)$ are second- and third-order loop filters respectively. Typical coefficients for the second- and third-order loop filters are $a_2 = 1.414$; $w_{0,2} = 4\times B_{w,2}\times a_2/[(a_2)^2+1]$; $a_3 = 1.1$; $b_3 = 2.4$; $w_{0,3} = B_{w,3}/0.7845$. $B_{w,2}$ and $B_{w,3}$ are the second- and third-order tracking loop bandwidths accordingly.

As stated earlier, three error sources are considered for static receivers. Using the clock error models described



▲ **FIGURE 4** Tracking loop performance analysis for 2- and 1-Hz loop bandwidth.

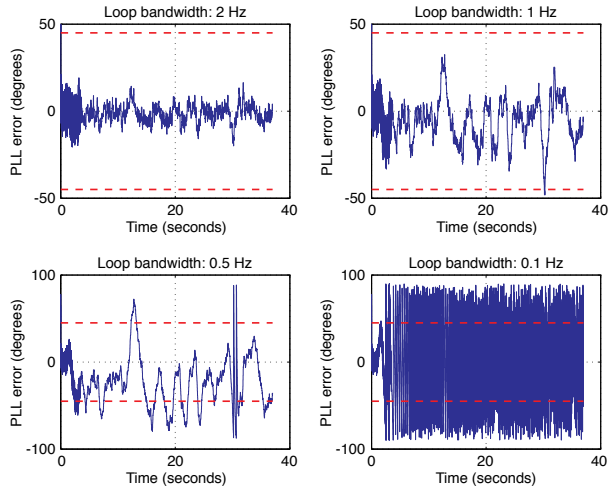
earlier, the contribution of different error sources to phase jitter is a function of PLL tracking bandwidth. The resulting phase tracking errors from different error sources are evaluated based on Equation (3) and shown in FIGURE 3.

The third-order PLL performance using 2-, 1-, 0.5- and 0.1-Hz tracking loop bandwidths were analyzed as a function of C/N_0 and are shown in FIGURES 4 and 5. For each selected bandwidth, three different qualities of receiver clocks were analyzed, and a conventional 15-degree performance threshold was adopted. The second-order PLL performs similarly to the third-order PLL. However, the phase jitter tends to be more biased when the tracking loop bandwidth becomes smaller. This phenomenon will be observed later on using signal data for performance validation. Therefore, only the third-order loop performance analysis is shown in Figures 4 and 5. It is obvious from these two figures that the minimum tracking loop bandwidth for a TCXO receiver PLL is about 2 Hz, and the PLL can work properly only while C/N_0 is above 24 dB-Hz.

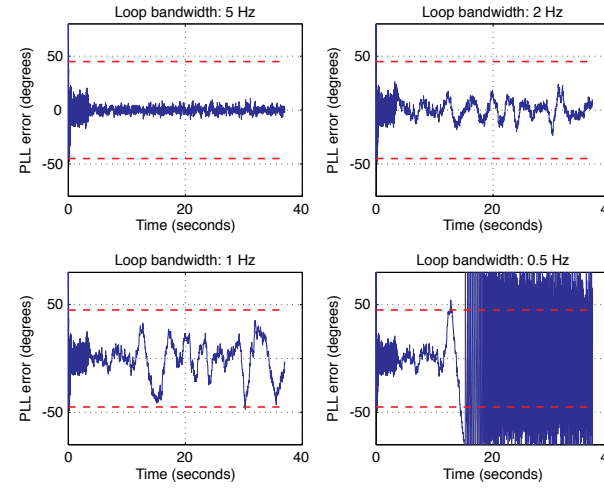
As for the receiver using atomic clocks, CSAC and a rubidium frequency standard in our analysis, the PLL bandwidth can be reduced down to at least 0.1 Hz while C/N_0 is above 15 dB-Hz.

Experimental Tracking Loop Performance

Experimental data were collected at Nottingham Scientific Limited. The experiment was conducted using a GPS/GNSS RF front end with a built-in TCXO clock. The RF front end also has the capability of accepting atomic clock signals through an external clock input connector to which the CSAC (see PHOTO) was connected during data collection. All data (using the built-in TCXO clock or the CSAC) were sampled at a 26-MHz sampling rate and at a 6.5-MHz IF with 2-MHz front-end bandwidth and four quantization levels.



▲ **FIGURE 6** Second-order PLL phase jitter using TCXO.



▲ **FIGURE 7** Third-order PLL phase jitter using TCXO.

A MatLab-coded software defined receiver (SDR) was used to process collected IF samples for tracking loop performance validation. TCXO phase jitters resulting from different tracking loop bandwidths are shown in FIGURE 6 for a typical second-order PLL under a nominal C/N_0, which is about 45 dB-Hz. A 45-degree loss-of-lock threshold was adopted (three times larger than the standard deviation threshold used in an earlier performance analysis). In our work, all code tracking delay lock loops (DLLs) are implemented using a second-order loop filter with 20-millisecond coherent integration time and 0.5-Hz loop bandwidth without any aiding. The resulting phase jitters in the figure become biased when the tracking loop bandwidth is reduced. This observed phenomenon implies that a second-order PLL time response cannot track the clock dynamics when the loop bandwidth approaches the minimum loop bandwidth (where loss of lock occurs).

The same IF data was re-processed by the SDR using the third-order PLL with the same range of tracking loop bandwidths. The resulting phase jitters are shown in FIGURES 7 and 8. There is no observable phase jitter bias before the PLLs lose lock in the figures. These results demonstrate that a third-order PLL performs better in terms of capturing the clock dynamics when the tracking loop bandwidth is reduced close to the limitation. Therefore, only the third-order PLL will be considered further.

The performance of the TCXO PLL can be evaluated from the results in Figure 7. It demonstrates that the minimum loop bandwidth is 2 Hz, which is consistent with the previous analysis shown in Figure 4. However, the minimum bandwidth using the CSAC is shown to be 0.5 Hz in Figure 8. This result does not meet the performance predicted by the analysis, which shows that the working bandwidth can be reduced to 0.1 Hz.

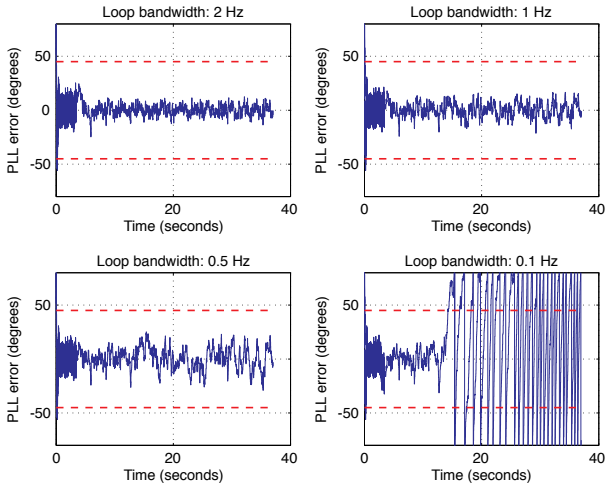
Analysis and Tracking Performance Under PPD Interference

The motivation of our work, as described earlier, is to improve the receiver signal tracking performance under PPD interference, or equivalently, wideband interference. We carried out a simple analysis first to understand how much signal deterioration a GBAS ground receiver could expect. A 13-dBm/MHz PPD currently available on the market was used to analyze the signal deterioration based on the distance between the PPD and the GBAS ground receiver. A simple analysis using a direct-path model shows that noise power roughly 30 dB higher than the nominal noise level (about -202 dBW/Hz) could be experienced by the GBAS ground receiver if the nearest distance is assumed to be 0.5 kilometers. In this case, any wideband interference mitigation method to address PPD interference has to handle C/N_0 as low as 10 to 15 dB-Hz.

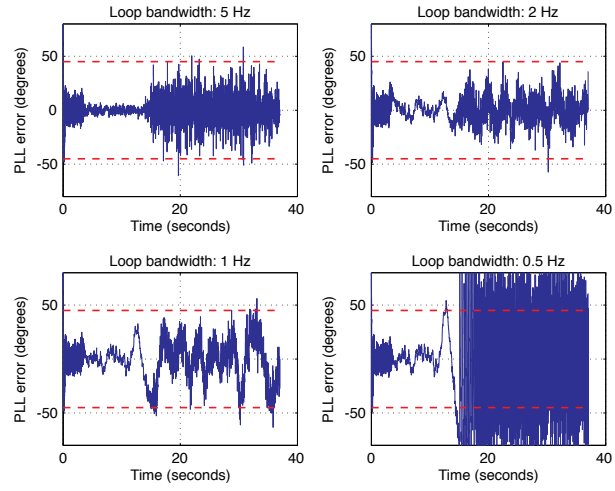
Gaussian distributed white noises were simulated and added on top of the original IF samples, then re-quantized to the original four quantization levels to mimic the PPD interference signal condition. A 20-dB higher noise level was simulated to demonstrate the effectiveness of this signal deterioration technique.

The tracking loop performance using the third-order PLL under low C/N_0 conditions was evaluated using the IF sampling and PPD interference simulation technique just described. The evaluation results show that the minimum PLL bandwidth using the TCXO is still 2 Hz. This result is roughly consistent with a previous analysis showing a 24-dB-Hz C/N_0 limitation using 2-Hz tracking bandwidth. The PLL using the CSAC performs better than that using the TCXO, which is expected.

After raising the noise level 5 dB higher to achieve an average of C/N_0 of 18 dB-Hz, phase jitters using the TCXO exceed the threshold at all bandwidths as shown



▲ **FIGURE 8** Third-order PLL phase jitter using CSAC.



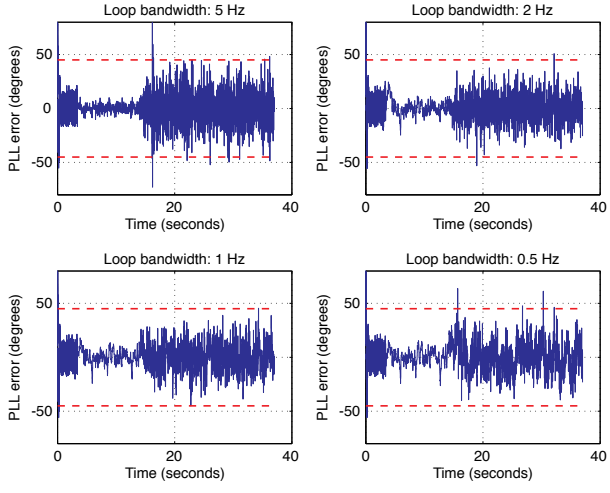
▲ **FIGURE 9** Phase jitter using TCXO under 18 dB-Hz C/N_0.

in FIGURE 9. The same magnitude of noise was also added to the CSAC IF samples. The resulting phase jitters are shown in FIGURE 10, which demonstrates that the minimum bandwidth is 1 Hz for this deteriorated signal condition. Any further increase in noise level will result in loss of lock for PLLs using a CSAC at all tracking bandwidths.

Summary and Future Work

We explored a baseband approach for an effective wideband interference mitigation method in this article. We have presented the theoretical analysis and actual data validation to study the possible improvement of the PLL tracking performance under PPD interference, which has been experienced by LAAS ground receivers.

The limitations of reducing PLL tracking loop bandwidths using different qualities of receiver clocks have been analyzed and compared with the experimental results generated by processing IF samples using an SDR. We conclude that the PLL tracking performance using a TCXO is consistent between theoretical prediction and data validation under both nominal and low C/N_0 conditions. However, the PLL tracking performance using the CSAC was not as good as the analysis prediction under both conditions.



▲ **FIGURE 10** Phase jitter using CSAC under 18 dB-Hz C/N_0.

In our future work, to understand the reason for the tracking performance inconsistency using the CSAC, we will carefully examine and evaluate the hardware components in line between the external clock input and the IF sampling chip. In this way, we will exclude the clock performance degradation due to any hardware incompatibility.

Other types of high quality clocks, such as extra-low-phase-noise oven-controlled crystal oscillators and low-phase-noise rubidium oscillators, will also be tested to explore the limitation of PLL tracking bandwidth reduction. If the results using other clocks exhibit good consistency between performance analysis and data validation, it is highly possible that the CSAC clock error model mis-represents the available commercial products.

In our future work, we will also consider simulating PPD interference more closely to the real scenario, by adding analog interference signals on top of GPS/GNSS analog signals before taking digital IF samples.

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Manufacturers

The CSAC used in our tests is a Symmetricom Inc., now part of **Microsemi Corp.** (*www.microsemi.com*), model SA.45s. We used a **Nottingham Scientific Ltd.** (*www.nsl.eu.com*) Stereo GPS/GNSS RF front end with the MatLab-based SoftGNSS 3.0 software from the **Danish GPS Center** at Aalborg University (*gps.aau.dk*).

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